In The Claims

Applicant submits below a complete listing of the current claims, with any insertions indicated by underlining and any deletions indicated by strikeouts and/or double bracketing.

This listing of claims will replace all prior versions, and listings, of claims in the application:

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Listing of the Claims

1. (Currently amended) A method for timing random reading of a memory device with a data access time, said reading being made up of a succession of consecutive operations, wherein each of said operations has, whatever the operating condition of said memory device, a fixed predetermined duration such as to guarantee completion of the operation within said fixed predetermined ~~durationin~~ ~~duration in~~ the worst operating condition of said memory device, the sum of the fixed predetermined ~~durationsof~~ durations of said operations being equal to said data access time of said memory device.

2. (Original) The timing method according to claim 1, wherein each of said operations making up said reading is started immediately at an end of the preceding operation.

3. (Original) The timing method according to claim 1, wherein said fixed predetermined duration is assigned to the corresponding operation in a design stage of said memory device.

4. (Original) The timing method according to claim 1, wherein each of said operations has a fixed predetermined duration, which is irrespective of the temperature variations of said memory device.

5. (Original) The timing method according to claim 1, wherein each of said operations has a fixed predetermined time duration, which is irrespective of the variations in a supply voltage of said memory device.

6. (Original) A device for timing random reading of a memory device with a data access time, said reading being made up of a succession of consecutive operations, said timing device comprising signal generating means, designed to generate, for each said operation, a corresponding timing signal such as to cause, whatever the operating condition of said memory device, the corresponding operation to last for a fixed predetermined duration such as to guarantee completion of said operation in the worst operating condition of said memory device, the sum of the durations of said operations being equal to said data access time of said memory device.

7. (Original) The timing device according to claim 6, wherein said signal generating means comprise a plurality of timing blocks, each of which generates a timing signal designed to drive termination of the respective operation, and is supplied at input to a timing block associated to a subsequent operation, for driving start of the latter.

8. (Original) The timing device according to claim 7, wherein each timing block comprises at least one input receiving a current which is constant and is irrespective of variations in temperature and supply voltage of said memory device, and at least one output supplying said timing signal.

9. (Original) The timing device according to claim 8, wherein said signal generating means further comprise at least one voltage generating block having an output connected to said input of said timing blocks for supplying the timing blocks with said constant current.

10. (Original) The timing device according to claim 9, wherein said voltage generating block comprises at least one NMOS cascode transistor and a resistor manufactured using an n-well technology.

11. (Original) The timing device according to claim 10, wherein said voltage generating block comprises a supply line set at the supply voltage; a ground line set at the ground voltage; at least one PMOS transistor connected to said output and to said supply line, said

resistor being connected to said ground line, and said NMOS transistor being arranged between said PMOS transistor and said resistor.

12. (Original) The timing device according to claim 10, wherein said NMOS transistor has a gate terminal set at a constant gate voltage, a source terminal connected to said resistor, and a drain terminal connected to the drain terminal of said PMOS transistor.

13. (Original) The timing device according to claim 6, wherein each timing block comprises a supply line set at the supply voltage; a ground line set at the ground voltage; a signal generator stage, which is designed to generate said timing signal having a fixed duration correlated to the fixed predetermined time of a respective operation; and a time duration regulation stage, which is designed to regulate said duration of said timing signal and is connected in series to said signal generator stage between said supply line and said ground line.

14. (Original) The timing device according to claim 13, wherein said signal generator stage and said duration regulating branch are connected to said constant current input so as to define with the voltage generating block a current mirror.

15. (Original) The timing device according to claim 14, wherein said signal generator stage comprises at least one NMOS cascode transistor.

16. (Original) The timing device according to claim 13, wherein said duration regulating branch comprises a plurality of capacitors connected in parallel to one another, and a plurality of selector means, designed to connect selectively each said capacitor to said duration regulating branch.

17. (Original) The timing device according to claim 16, wherein said signal generator stage comprises at least one PMOS transistor connected to said supply line, at least one NMOS transistor connected to said NMOS transistor at an intermediate node, and at least one logic gate arranged between said intermediate node and said output.